UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,945	10/29/2003	Vasudevan Parthasarathy	1875.5430000	6137

26111 7590 04/03/2007

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ETTEHADIEH, ASLAN	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,945	PARTHASARATHY, VASUDEVAN	
	Examiner	Art Unit	
	Aslan Ettehadieh	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1 – 20 (group 1) in the reply filed on 02/23/2007 is acknowledged. Claims 21 – 23 are now cancelled. Office action address claims 1 – 20.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings are objected to because figure 14 and paragraphs 70 – 71 disclose a serial to parallel element, however, the input to the element shows a bidirectional communication on the left of the element and a serial stream on the right, if data is moving from the left to the right, should a serial data stream produce a parallel data stream. Also, serializing the inverted differential data signal is not shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and

where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 1 is objected to because of the following informalities: please change "a valid data word" to "the valid data word" in the last limitation of claim 1.

5. Claim 2 is objected to because of the following informalities: please change "said data differential data" to "said differential data".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4 – 6, 10 – 13, are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida (US 5903613).

7. Regarding claim 1, Ishida discloses a method of processing a data signal, comprising: receiving a differential data signal (col. 1 lines 7 – 10, 12 – 13, 66 – 67, col. 2 lines 1 – 5; where a differential signal is being interpreted as a differential data signal

because the differential signal is received by a data reception device); determining if said differential data signal represents a valid data word (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 21 – 29); and if said differential data signal does not represent a valid data word, then inverting said differential data signal, producing an inverted differential data signal (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 37 – 42; where reversing the polarities is being interpreted as inverting).

8. Regarding claim 4, Ishida further discloses the step of further processing said inverted differential data signal (figure 1 element 103, figures 9, 13).

9. Regarding claim 5, Ishida further discloses the step of serializing said inverted differential data signal (figure 1 element 108, figures 9, 13).

10. Regarding claim 6, Ishida further discloses comprising the step of transmitting the result of said serializing step to a destination node (figure 21; where element 2114 is the data reception device as also in figures 1, 9, 13; and where a destination node could be numerous elements of figure 21, i.e. element 2102, 2120)

11. Regarding claim 10, Ishida further discloses the step of determining if said inverted differential data signal represents a valid data word (col. 10 line 41 – 59, figure 1 elements 104, 109, 102).

12. Regarding claim 11, Ishida further discloses further comprising the step of further processing said inverted differential data signal if said inverted differential data signal represents a valid data word (figure 1 element 103, figures 9, 13).

13. Regarding claim 12, Ishida further discloses wherein said differential data signal includes a first component and a second component, and wherein said step of inverting

comprises the step of inverting a logic state of said first component of said differential data signal, and inverting a logic state of said second component of said differential data signal (col. 1 line 66 – col. 2 line 67).

14. Regarding claim 13, Ishida discloses a method of processing a data signal, comprising: receiving a differential data signal having a first component and a second component (col. 1 lines 7 – 10, 12 – 13, 66 – 67, col. 2 lines 1 – 5; where a differential signal is being interpreted as a differential data signal because the differential signal is received by a data reception device); comparing a data word represented by said differential data signal with one or more valid data words (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 21 – 29); and if said data word of said differential data signal is not consistent with at least one of said one or more valid data words, then inverting said first component and said second component of said differential data signal, producing an inverted differential data signal (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 37 – 42; where reversing the polarities is being interpreted as inverting).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 7 – 8, 15, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida (US 5903613).

16. Regarding claim 7, Ishida further discloses wherein said step of determining comprises the step of comparing a data word represented by said differential data signal with one or more valid data words stored in a memory (col. 1 line 66 – col. 2 line 67; where it would have been obvious to one skilled in the art at the time of invention was made to have the 00 or 11 stored by a memory to save processing time).

17. Regarding claim 8, Ishida further discloses the step of generating a control signal based on said step of comparing (col, 1 line 66 – col. 2 line 67; it would have been obvious to one skilled in the art at the time of invention was made to have a control function, i.e. control signal for after the detection of the error(s) to instruct the function of polarity reversing to occur in order for the system to properly correct the error).

18. Regarding claim 15, Ishida discloses a transceiver, comprising: a receiver input for receiving a serial data signal (col. 1 lines 7 – 10, 12 – 13, 66 – 67, col. 2 lines 1 – 5); providing parallel signals (figure 1); an error check for determining if a differential output of parallel inputs represents a valid data word (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 21 – 29); and a logic circuit for inverting said differential output if said differential output does not represent a valid data word (col. 1 line 66 – col. 2 line 67, particularly col. 2 lines 37 – 42; where reversing the polarities is being interpreted as inverting). Ishida is not explicit about a serial-to-parallel converter coupled to an output of said receiver input, however, figure 1 shows a parallel stream and it would have been obvious to one skilled in the art at the time of invention was made to use a serial-to-parallel converter coupled to an output of said receiver input in order to processes data in parallel and simultaneously thus saving processing time).

19. Regarding claim 19, Ishida further discloses wherein said error check includes a memory that stores one or more valid data words, and wherein said error check generates said control signal based on a comparison between said differential output and said one or more valid code words (col. 1 line 66 – col. 2 line 67; where it would have been obvious to one skilled in the art at the time of invention was made to have the 00 or 11 stored by a memory to save processing time and col. 1 line 66 – col. 2 line 67; it would have been obvious to one skilled in the art at the time of invention was made to have a control function, i.e. control signal for after the detection of the error(s) to instruct the function of polarity reversing to occur in order for the system to properly correct the error).

20. Claims 1 – 3, 13 – 14, 16 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takami (US 2004/0153945).

21. Regarding claims 1, 13 and 15, Takami discloses a method and apparatus of a transceiver processing a data signal, comprising a receiver input for receiving a serial data signal; a serial-to-parallel converter coupled to an output of said receiver input (figure 1, paragraph 4); an error check for determining if a differential output of said serial-to-parallel converter represents a valid data word (figure 1, paragraphs 4, 11 – 12, 23, 25, 27, 29, abstract); and a logic circuit for inverting said differential output if said differential output does not represent a valid data word (figure 1, paragraphs 4, 11 – 12, 23, 25, 27, 29, abstract). Takami does not disclose a differential data signal having a first component and a second component, however, it would have been obvious to one

skilled in the art at the time of invention was made to use differential data signal having a first component and a second component in the system of Takami because a differential signal has the advantage of allowing faster data rates because the differential signals traverse lower voltage swings than single ended signals. Also, the data is less susceptible to noise in a differential signal bus because common mode signal noise picked up on the transmission cable is cancelled by sensing only the difference between the positive and negative conductors of the cable.

22. Regarding claims 2 and 3, Takami further discloses wherein said step of inverting includes the step of X-ORing said differential data signal with a control bit, said control bit being a logic "1" if said differential data signal represents an invalid data word; and wherein said control bit is a logic "0" if said differential data signal represents a valid data word (paragraph 29).

23. Regarding claim 14, Takami further discloses generating a control signal if said data word of said data signal is not consistent with at least one of said one or more valid data words, said control signal having a logic state "1"; and X-ORing said control signal with said first and second components of said data signal to produce said inverted data signal (paragraph 29).

24. Regarding claim 16, Takami further discloses wherein said logic circuit includes a X-OR circuit having said differential output as a first input and a control signal as a second input (paragraph 29, figure 1).

25. Regarding claim 17, Takami further discloses wherein said control signal causes said X-OR circuit to invert said differential output of said serial-to-parallel converter if said differential output does not represent a valid data word (paragraph 29, figure 1).

26. Regarding claim 18, Takami further discloses wherein said control signal is a logic "1" if said differential output does not represent a valid data word, and said control signal is a logic "0" if said differential output represents a valid data word (paragraph 29, figure 1).

27. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takami (US 2004/0153945) in view of Saliba (US 2004/0181734).

28. Regarding claim 7, Takamiis silent about disclosing wherein said step of determining comprises the step of comparing a data word represented by said data signal with one or more valid data words stored in a memory.

In the same field of endeavor, however, Saliba discloses wherein said step of determining comprises the step of comparing a data word represented by said data signal with one or more valid data words stored in a memory (paragraphs 39 – 40).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use wherein said step of determining comprises the step of comparing a data word represented by said data signal with one or more valid data words stored in a memory as taught by Saliba in the system of Takami to reduce the processing time by only recalling from memory what is needed and not reprocessing data at every iteration.

29. Regarding claim 9, Takami further discloses wherein said control signal represents a logic "1" if said data word represented by said differential data signal is not consistent with at least one of said valid data words, and wherein said control signal represents a logic "0" if said data word is consistent with at least one of said one or more valid data words (paragraph 29).

30. Claims 19 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takami (US 2004/0153945) in view of Kim et al. (US 6820232)

31. Regarding claim 19, Takami is not explicit about wherein said error check includes a memory that stores one or more valid data words, and wherein said error check generates said control signal based on a comparison between said differential output and said one or more valid code words (paragraphs 7, 10).

In the same field of endeavor, however, Kim discloses wherein said error check includes a memory that stores one or more valid data words, and wherein said error check generates said control signal based on a comparison between said differential output and said one or more valid code words (abstract, col. 3 lines 23 – 41, col. 4 lines 1 – 57, col. 5 lines 32 – 46, col. 6 lines 11 – 44).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use wherein said error check includes a memory that stores one or more valid data words, and wherein said error check generates said control signal based on a comparison between said differential output and said one or more valid code words as taught by Kim in the system of Takami to properly detect errors.

32. Regarding claim 20, Takami further discloses wherein said error check generates said control signal to have a logic "1" if said differential output is not consistent with at least one of said valid code words (paragraph 29).

Other prior art cited

The prior art made of record and not relies upon is considered pertinent to applicant's disclosure.

33. Chang et al. (US 20030057932) discloses all limitations in claims 1 and 13 (abstract, figures 3 and 4, paragraphs 2 – 5, 8 – 9, 17, 19, 21 – 23). Chang also discloses the use of a control signal (paragraph 23).

34. Farnsworth (US 2005/0086571) discloses a system of relevance to claimed invention (paragraphs 46 – 53)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aslan Ettehadieh
Examiner
Art Unit 2611

AE

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER